

Features

- Fast Read Access Time - 70 ns
- Low Power CMOS Operation
 - 100 μ A max. Standby
 - 30 mA max. Active at 5 MHz
- JEDEC Standard Packages
 - 32-Lead 600-mil PDIP
 - 32-Lead 450-mil SOIC (SOP)
 - 32-Lead PLCC
 - 32-Lead TSOP
- 5V \pm 10% Supply
- High Reliability CMOS Technology
 - 2000V ESD Protection
 - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 μ s/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27C040 chip is a low-power, high-performance, 4,194,304-bit one-time programmable read only memory (OTP EPROM) organized as 512K by 8 bits. The AT27C040 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 70 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

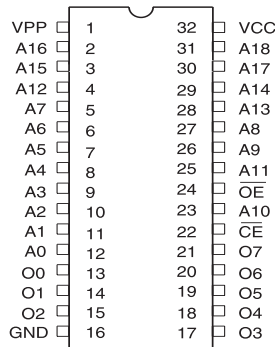
Atmel's scaled CMOS technology provides low active power consumption, and fast programming. Power consumption is typically 8 mA in active mode and less than 10 μ A in standby mode.

(continued)

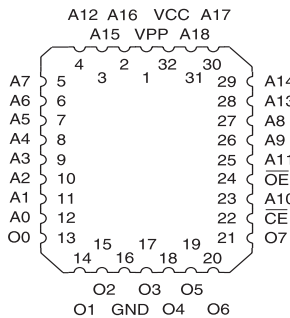
Pin Configurations

| Pin Name | Function |
|-----------------|---------------|
| A0 - A18 | Addresses |
| O0 - O7 | Outputs |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |

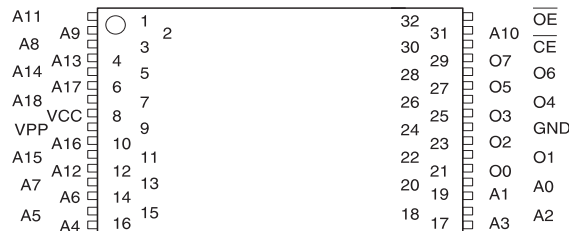
PDIP, SOIC Top View



PLCC Top View



TSOP Top View



4-Megabit (512K x 8) OTP EPROM

AT27C040





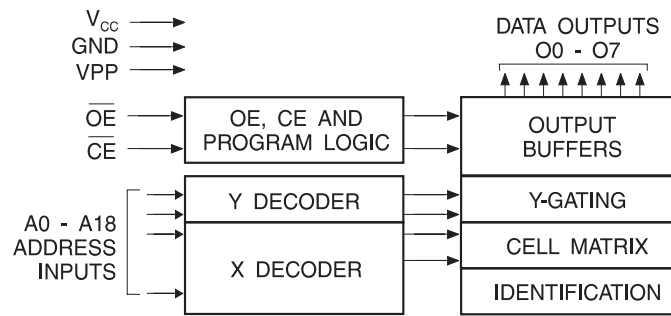
The AT27C040 is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, SOIC (SOP), and TSOP packages. The device features two-line control (\overline{CE} , \overline{OE}) to eliminate bus contention in high-speed systems.

Atmel's AT27C040 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 μs /byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Switching Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 μF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Operating Modes

| Mode/Pin | CE | OE | Ai | V _{PP} | Outputs |
|---------------------------------------|-----------------|-----------------|---|------------------|---------------------|
| Read | V _{IL} | V _{IL} | Ai | X ⁽¹⁾ | D _{OUT} |
| Output Disable | X | V _{IH} | X | X | High Z |
| Standby | V _{IH} | X | X | X | High Z |
| Rapid Program ⁽²⁾ | V _{IL} | V _{IH} | Ai | V _{PP} | D _{IN} |
| PGM Verify | X | V _{IL} | Ai | V _{PP} | D _{OUT} |
| PGM Inhibit | V _{IH} | V _{IH} | X | V _{PP} | High Z |
| Product Identification ⁽⁴⁾ | V _{IL} | V _{IL} | A9 = V _H ⁽³⁾ A0 = V _{IH} or V _{IL} A1 - A18 = V _{IL} | X | Identification Code |

Notes: 1. X can be V_{IL} or V_{IH}.

2. Refer to Programming Characteristics

3. V_H = 12.0 ± 0.5V.

4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

Absolute Maximum Ratings*

| | |
|--|--------------------------------|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature..... | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V ⁽¹⁾ |
| Voltage on A9 with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |
| V _{PP} Supply Voltage with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



DC and AC Operating Conditions for Read Operation

| | | AT27C040 | | | |
|------------------------------|------|--------------|--------------|--------------|--------------|
| | | -70 | -90 | -12 | -15 |
| Operating Temperature (Case) | Com. | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C |
| | Ind. | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C |
| V _{CC} Power Supply | | 5V ± 10% | 5V ± 10% | 5V ± 10% | 5V ± 10% |

DC and Operating Characteristics for Read Operation

| Symbol | Parameter | Condition | Min | Max | Units |
|---------------------------------|---|---|------|-----------------------|-------|
| I _{LI} | Input Load Current | V _{IN} = 0V to V _{CC} | | ±1 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} = 0V to V _{CC} | | ±5 | μA |
| I _{PP1} ⁽²⁾ | V _{PP} ⁽¹⁾ Read/Standby Current | V _{PP} = V _{CC} | | 10 | μA |
| I _{SB} | V _{CC1} ⁽¹⁾ Standby Current | I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$ | | 100 | μA |
| | | I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V | | 1 | mA |
| I _{CC} | V _{CC} Active Current | f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$ | | 30 | mA |
| V _{IL} | Input Low Voltage | | -0.6 | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.0 | V _{CC} + 0.5 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA | | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -400 μA | 2.4 | | V |

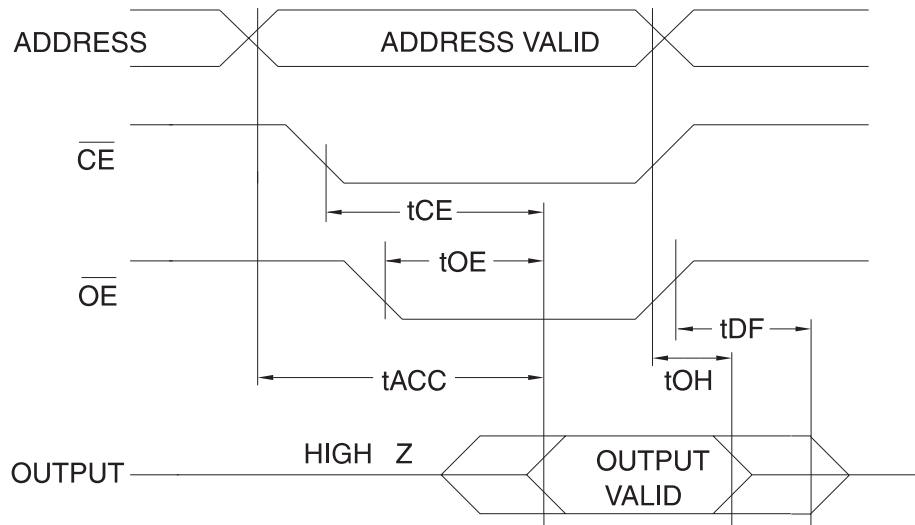
- Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}
 2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}

AC Characteristics for Read Operation

| Symbol | Parameter | Condition | AT27C040 | | | | | | | | Units |
|-----------------------------------|---|--|----------|-----|-----|-----|-----|-----|-----|-----|-------|
| | | | -70 | | -90 | | -12 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t _{ACC} ⁽³⁾ | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ | | 70 | | 90 | | 120 | | 150 | ns |
| t _{CE} ⁽²⁾ | \overline{CE} to Output Delay | $\overline{OE} = V_{IL}$ | | 70 | | 90 | | 120 | | 150 | ns |
| t _{OE} ⁽²⁾⁽³⁾ | \overline{OE} to Output Delay | $\overline{CE} = V_{IL}$ | | 30 | | 35 | | 35 | | 40 | ns |
| t _{DF} ⁽⁴⁾⁽⁵⁾ | \overline{OE} or \overline{CE} High to Output Float, whichever occurred first | | | 20 | | 20 | | 30 | | 30 | ns |
| t _{OH} | Output Hold from Address, \overline{CE} or \overline{OE} , whichever occurred first | | 0 | | 0 | | 0 | | 0 | | ns |

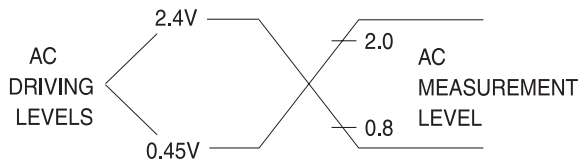
- Note: 2, 3, 4, 5 - see AC Waveforms for Read Operation

AC Waveforms for Read Operation⁽¹⁾

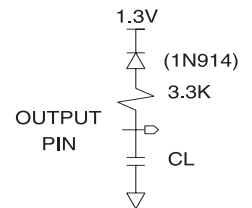


- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
 2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .
 3. \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC} .
 4. This parameter is only sampled and is not 100% tested.
 5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



Output Test Load



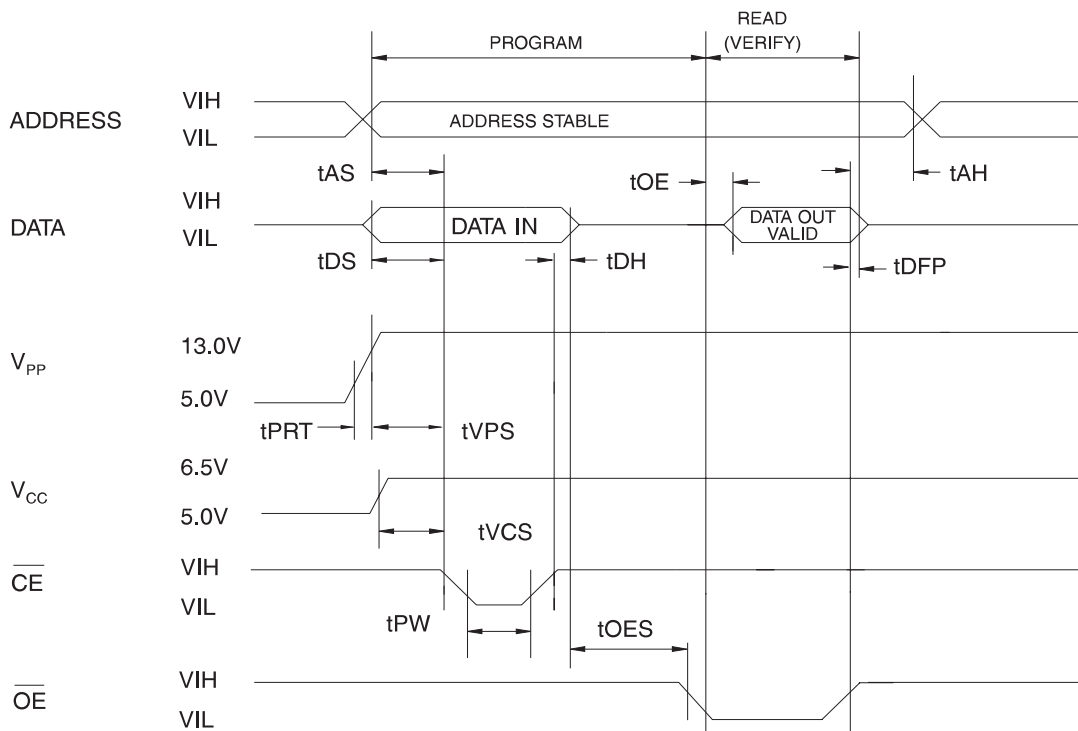
Pin Capacitance

($f = 1 \text{ MHz}$, $T = 25^\circ\text{C}$)⁽¹⁾

| | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 4 | 8 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 8 | 12 | pF | $V_{OUT} = 0V$ |

- Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms⁽¹⁾



- Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH} .
 2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
 3. When programming the AT27C040 a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

| Symbol | Parameter | Test Conditions | Limits | | Units |
|-----------|--|-----------------------------|--------|----------------|---------------|
| | | | Min | Max | |
| I_{LI} | Input Load Current | $V_{IN} = V_{IL}, V_{IH}$ | | ± 10 | μA |
| V_{IL} | Input Low Level | | -0.6 | 0.8 | V |
| V_{IH} | Input High Level | | 2.0 | $V_{CC} + 0.7$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1 \text{ mA}$ | | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -400 \mu\text{A}$ | 2.4 | | V |
| I_{CC2} | V_{CC} Supply Current (Program and Verify) | | | 40 | mA |
| I_{PP2} | V_{PP} Supply Current | $\overline{CE} = V_{IL}$ | | 20 | mA |
| V_{ID} | A9 Product Identification Voltage | | 11.5 | 12.5 | V |

AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Limits | | Units |
|-----------|---|--|--------|-----|---------------|
| | | | Min | Max | |
| t_{AS} | Address Setup Time | Input Rise and Fall Times (10% to 90%) 20ns | 2 | | μs |
| t_{OES} | \overline{OE} Setup Time | | 2 | | μs |
| t_{DS} | Data Setup Time | | 2 | | μs |
| t_{AH} | Address Hold Time | Input Pulse Levels 0.45V to 2.4V | 0 | | μs |
| t_{DH} | Data Hold Time | | 2 | | μs |
| t_{DFP} | \overline{OE} High to Output Float Delay ⁽²⁾ | Input Timing Reference Level 0.8V to 2.0V | 0 | 130 | ns |
| t_{VPS} | V_{PP} Setup Time | | 2 | | μs |
| t_{VCS} | V_{CC} Setup Time | | 2 | | μs |
| t_{PW} | \overline{CE} Program Pulse Width ⁽³⁾ | Output Timing Reference Level 0.8V to 2.0V | 95 | 105 | μs |
| t_{OE} | Data Valid from \overline{OE} ⁽²⁾ | | | 150 | ns |
| t_{PRT} | V_{PP} Pulse Rise Time During Programming | | 50 | | ns |

- Notes:
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}
 - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
 - Program Pulse width tolerance is $100 \mu\text{sec} \pm 5\%$.

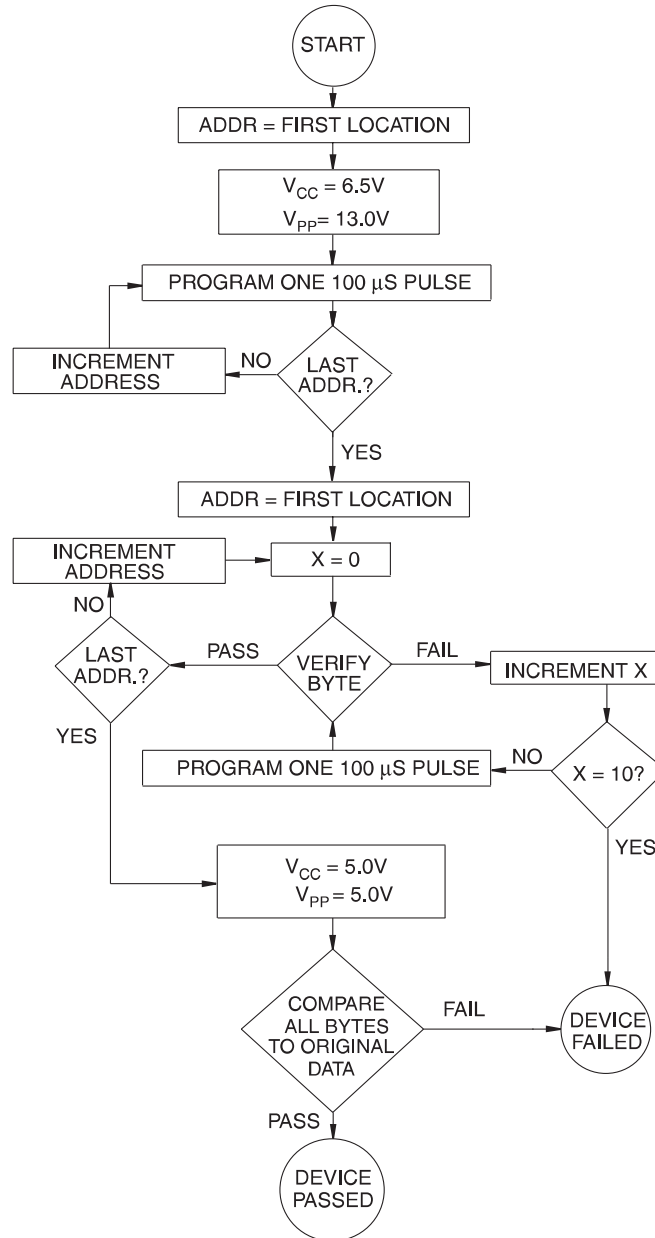
Atmel's 27C040 Integrated Product Identification Code

| Codes | Pins | | | | | | | | | Hex Data |
|--------------|------|----|----|----|----|----|----|----|----|----------|
| | A0 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | |
| Manufacturer | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E |
| Device Type | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B |

Rapid Programming Algorithm

A 100 μs $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 μs $\overline{\text{CE}}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 μs pulses are applied with a verification after each

pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

| t _{ACC} (ns) | I _{CC} (mA) | | Ordering Code | Package | Operation Range |
|-----------------------|----------------------|---------|--|---------------------------|-------------------------------|
| | Active | Standby | | | |
| 70 | 30 | 0.1 | AT27C040-70JC AT27C040-70PC AT27C040-70RC AT27C040-70TC | 32J 32P6 32R 32T | Commercial (0°C to 70°C) |
| | 30 | 0.1 | AT27C040-70JI AT27C040-70PI AT27C040-70RI AT27C040-70TI | 32J 32P6 32R 32T | Industrial (-40°C to 85°C) |
| 90 | 30 | 0.1 | AT27C040-90JC AT27C040-90PC AT27C040-90RC AT27C040-90TC | 32J 32P6 32R 32T | Commercial (0°C to 70°C) |
| | 30 | 0.1 | AT27C040-90JI AT27C040-90PI AT27C040-90RI AT27C040-90TI | 32J 32P6 32R 32T | Industrial (-40°C to 85°C) |
| 120 | 30 | 0.1 | AT27C040-12JC AT27C040-12PC AT27C040-12RC AT27C040-12TC | 32J 32P6 32R 32T | Commercial (0°C to 70°C) |
| | 30 | 0.1 | AT27C040-12JI AT27C040-12PI AT27C040-12RI AT27C040-12TI | 32J 32P6 32R 32T | Industrial (-40°C to 85°C) |
| 150 | 30 | 0.1 | AT27C040-15JC AT27C040-15PC AT27C040-15RC AT27C040-15TC | 32J 32P6 32R 32T | Commercial (0°C to 70°C) |
| | 30 | 0.1 | AT27C040-15JI AT27C040-15PI AT27C040-15RI AT27C040-15TI | 32J 32P6 32R 32T | Industrial (-40°C to 85°C) |

| Package Type | |
|--------------|--|
| 32J | 32-Lead, Plastic J-Leaded Chip Carrier (PLCC) |
| 32P6 | 32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| 32R | 32-Lead, 0.450" Wide, Plastic Gull Wing Small Outline (SOIC) |
| 32T | 32-Lead, Plastic Thin Small Outline Package (TSOP) |

This datasheet has been downloaded from:

www.DatasheetCatalog.com

Datasheets for electronic components.